UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,411	07/22/2003	Sohei Manabe	38493-8064US	8143

25096 7590 07/19/2005

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
LE, QUE TAN	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,411	MANABE ET AL.	
	Examiner	Art Unit	
	Que T. Le	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 November 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-16 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The present specification fails to provide a clear indication and/or discussion regarding "a depletion mode MOSFET", "an N-type MOSFET" and/or P-type MOSFET" as being claimed.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 17 is rejected under 35 U.S.C. 102(b) as being anticipated by Yang et al 6,180,969.

Yang et al disclose a well known active pixel for use in a CMOS image sensor system comprising a pinned photodiode (34), a depletion mode transistor (35a) for selectively transferring charge from the pinned photodiode to an output node (37); and a reset transistor (35b) coupled to the output node to reset the output node to a reset voltage during a reset period.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al 6,180,969.

With respect to claims 1, 3, 7, 8 and 20, note that Yang et al disclose an improvement image sensing system by replacing the pinned photodiode with a low voltage photodiode (LVPD) and at least one depletion transistor (520) for transferring photoelectric charge and another depletion transistor (530) for resetting the output node. The system includes an output transistor (540) having the gate connected to the

output node and a select transistor (550) coupled to a select line. Yang et al fail to indicate whether or not the depletion mode transistors are MOSFETs and/or P-type MOSFETs. Since the use of pinned photodiode(s) for CMOS image sensing system is known in the art and the alternate use of another photodiode for the purposes of completing the depletion of the photodiode. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yang et al accordingly in order to minimize a possible dark current from the photodiode. The inclusion of depletion mode MOSFETs and/or P-type MOSFET(s) would have also been obvious as a matter of obvious selection without altering the basic performances of the transistors.

With respect to claim 2, although Yang et al fail to specify whether the select transistor is a row or a column select transistor, it would have been a row select transistor, however, if not, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yang et al accordingly in order to provide a desired selection for the system.

With respect to claims 4 and 18, although yang et al lack a clear inclusion of a negative voltage generator for turning on and/or off the transistors, it would have been inherently include as disclose at least in column 6, however, if not, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yang et al accordingly in order to provide a better control for the transistors of the system.

With respect to claims 5, 6 and 19, although Yang et al fail to specify a threshold voltage of the transistor, selecting a desired voltage for a depletion mode transistor for providing a specific operation of the transistor would have been obvious to one of

ordinary skill in the art. It would have been obvious to modify Yang et al accordingly in order to provide a more control to the performance of the transistors.

With respect to claims 9-16, although Yang et al lack a clear inclusion of a processing circuitry and an i/o circuit for the system, it would have been inherently included, however, if not, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yang et al accordingly in order to provide a further use of the output of the system. The inclusion of a row select transistor, a negative voltage and/or a threshold voltage would have been obvious for similar reasons set forth in the discussion above.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

I) Chi 6,064,053 discloses an active pixel sensor system having CMOS transistors with a reset circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Que T: Le whose telephone number is (571) 272-2438.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Porta, can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Que T. Le
Primary Examiner